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## WHAT IS CLAIMED IS:

1           1.    For use in a CDMA receiver, a noise reduction circuit for  
2   improving a signal-to-noise ratio of a received signal comprising  
3   a series of chip sequences, said noise reduction circuit  
4   comprising:

5                a sampling circuit capable of generating an original  
6   plurality of samples of said received signal; and

7                a controller capable of determining a first plurality of  
8   time slots, each of said first plurality of time slots comprising  
9   a plurality of chip samples corresponding to Logic 1, and a second  
10   plurality of time slots, each of said second plurality of time  
11   slots comprising a plurality of chip samples corresponding to  
12   Logic 0, wherein said controller is capable of generating a  
13   reconstructed plurality of samples by at least one of:

14                    modifying an order of a first Logic 1 chip sample  
15   and a second Logic 1 chip sample; and

16                    modifying an order of a first Logic 0 chip sample  
17   and a second Logic 0 chip sample.

1           2.    The noise reduction circuit set forth in Claim 1 wherein  
2    said controller adds said reconstructed plurality of samples and  
3    said original plurality of samples to generate a composite signal  
4    having a reduced signal-to-noise ratio.

1           3.    The noise reduction circuit set forth in Claim 1 wherein  
2    said CDMA receiver is a receiver in a base station of a wireless  
3    network.

1           4.    The noise reduction circuit set forth in Claim 1 wherein  
2    said CDMA receiver is a receiver in a mobile station capable of  
3    communicating with a wireless network.

1           5.    The noise reduction circuit set forth in Claim 1 wherein  
2    said first Logic 1 chip sample and said second Logic 1 chip sample  
3    are contained within a single chip.

1           6.    The noise reduction circuit set forth in Claim 1 wherein  
2    said first Logic 0 chip sample and said second Logic 0 chip sample  
3    are contained within a single chip.

1           7.    The noise reduction circuit set forth in Claim 1 wherein  
2   said first Logic 1 chip sample and said second Logic 1 chip sample  
3   are contained within different chips and said first Logic 0 chip  
4   sample and said second Logic 0 chip sample are contained within  
5   different chips.

1           8.    The noise reduction circuit set forth in Claim 1 wherein  
2   said controller one of modifies said order of said first and second  
3   Logic 1 chip samples and modifies said order of said first and  
4   second Logic 0 chip samples according to one of a random process  
5   algorithm and a predetermined algorithm.

1           9.    A CDMA wireless network comprising a plurality of base  
2    stations, each of said base stations comprising a noise reduction  
3    circuit for improving a signal-to-noise ratio of a received signal  
4    comprising a series of chip sequences, said noise reduction circuit  
5    comprising:

6                a sampling circuit capable of generating an original  
7    plurality of samples of said received signal; and

8                a controller capable of determining a first plurality of  
9    time slots, each of said first plurality of time slots comprising  
10   a plurality of chip samples corresponding to Logic 1, and a second  
11   plurality of time slots, each of said second plurality of time  
12   slots comprising a plurality of chip samples corresponding to  
13   Logic 0, wherein said controller is capable of generating a  
14   reconstructed plurality of samples by at least one of:

15                modifying an order of a first Logic 1 chip sample  
16   and a second Logic 1 chip sample; and

17                modifying an order of a first Logic 0 chip sample  
18   and a second Logic 0 chip sample.

1           10. The CDMA wireless network set forth in Claim 9 wherein  
2       said controller adds said reconstructed plurality of samples and  
3       said original plurality of samples to generate a composite signal  
4       having a reduced signal-to-noise ratio.

1           11. The CDMA wireless network set forth in Claim 9 wherein  
2       said first Logic 1 chip sample and said second Logic 1 chip sample  
3       are contained within a single chip.

1           12. The CDMA wireless network set forth in Claim 9 wherein  
2       said first Logic 0 chip sample and said second Logic 0 chip sample  
3       are contained within a single chip.

1           13. The CDMA wireless network set forth in Claim 9 wherein  
2       said first Logic 1 chip sample and said second Logic 1 chip sample  
3       are contained within different chips and said first Logic 0 chip  
4       sample and said second Logic 0 chip sample are contained within  
5       different chips.

1           14. The CDMA wireless network set forth in Claim 9 wherein  
2       said controller one of modifies said order of said first and second  
3       Logic 1 chip samples and modifies said order of said first and  
4       second Logic 0 chip samples according to one of a random process  
5       algorithm and a predetermined algorithm.

1        15. A wireless mobile station capable of communicating with  
2        a plurality of base stations in a wireless network, said wireless  
3        mobile station comprising a reduction circuit for improving a  
4        signal-to-noise ratio of a received signal comprising a series of  
5        chip sequences, said noise reduction circuit comprising:

6                a sampling circuit capable of generating an original  
7        plurality of samples of said received signal; and

8                a controller capable of determining a first plurality of  
9        time slots, each of said first plurality of time slots comprising  
10       a plurality of chip samples corresponding to Logic 1, and a second  
11       plurality of time slots, each of said second plurality of time  
12       slots comprising a plurality of chip samples corresponding to  
13       Logic 0, wherein said controller is capable of generating a  
14       reconstructed plurality of samples by at least one of:

15                modifying an order of a first Logic 1 chip sample  
16        and a second Logic 1 chip sample; and

17                modifying an order of a first Logic 0 chip sample  
18        and a second Logic 0 chip sample.



1        16. The wireless mobile station set forth in Claim 15 wherein  
2        said controller adds said reconstructed plurality of samples and  
3        said original plurality of samples to generate a composite signal  
4        having a reduced signal-to-noise ratio.

1        17. The wireless mobile station set forth in Claim 15 wherein  
2        said first Logic 1 chip sample and said second Logic 1 chip sample  
3        are contained within a single chip.

1        18. The wireless mobile station set forth in Claim 15 wherein  
2        said first Logic 0 chip sample and said second Logic 0 chip sample  
3        are contained within a single chip.

1        19. The wireless mobile station set forth in Claim 15 wherein  
2        said first Logic 1 chip sample and said second Logic 1 chip sample  
3        are contained within different chips and said first Logic 0 chip  
4        sample and said second Logic 0 chip sample are contained within  
5        different chips.

1           20. The wireless mobile station set forth in Claim 15 wherein  
2       said controller one of modifies said order of said first and second  
3       Logic 1 chip samples and modifies said order of said first and  
4       second Logic 0 chip samples according to one of a random process  
5       algorithm and a predetermined algorithm.

1           21. For use in a CDMA receiver, a method of improving a  
2 signal-to-noise ratio of a received signal comprising a series of  
3 chip sequences, the method comprising the steps of:

4           sampling the receiving signal to generate an original  
5 plurality of samples of the received signal;

6           determining a first plurality of time slots, each of the  
7 first plurality of time slots comprising a plurality of chip  
8 samples corresponding to Logic 1, and a second plurality of time  
9 slots, each of the second plurality of time slots comprising a  
10 plurality of chip samples corresponding to Logic 0; and

11           generating a reconstructed plurality of samples by at  
12 least one of:

13           modifying an order of a first Logic 1 chip sample  
14 and a second Logic 1 chip sample; and

15           modifying an order of a first Logic 0 chip sample  
16 and a second Logic 0 chip sample.

1           22. The method set forth in Claim 21 including the further  
2 step of adding the reconstructed plurality of samples and the  
3 original plurality of samples to generate a composite signal having  
4 a reduced signal-to-noise ratio.

1           23. The method set forth in Claim 21 wherein the first  
2       Logic 1 chip sample and the second Logic 1 chip sample are  
3       contained within a single chip.

1           24. The method set forth in Claim 21 wherein the first  
2       Logic 0 chip sample and the second Logic 0 chip sample are  
3       contained within a single chip.

1           25. The method set forth in Claim 21 wherein the first  
2       Logic 1 chip sample and the second Logic 1 chip sample are  
3       contained within different chips and the first Logic 0 chip sample  
4       and the second Logic 0 chip sample are contained within different  
5       chips.

1           26. The method set forth in Claim 1 wherein the sub-step of  
2       modifying the order of the first and second Logic 1 chip samples  
3       and the sub-step of modifying the order of the first and second  
4       Logic 0 chip samples are performed according to one of a random  
5       process algorithm and a predetermined algorithm.